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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,915	02/22/2002	Fernando Gonzalez	MCRO:125--4/FLE 94-0281.0	4617

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EXAMINER	
PERALTA, GINETTE	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/081,915	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-60* is/are pending in the application.

4a) Of the above claim(s) *18,21-34,37-39 and 50-52* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19,20,35-36,40-49,53-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 19, 20, 35, 36, 40-49, and 53-60 in Paper No. 7 is acknowledged. Claims 18, 21-34, 37-39, 50, and 51 are withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 19, 35, 36, and 40-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (U. S. Pat. 5,731,219) in view of Brickman et al. (U. S. Pat. 3,721,838), as applied before.

Ikeda et al. discloses in figs. 9, and 26-32, a method for making a memory device that comprises providing a substrate having a first conductive line 13 therein; forming a plurality of memory cells; forming a second conductive line 29, the second conductive line 29 in electrical communication with one of the memory cells; and creating a third conductive line 33 in electrical communication with the first conductive line and the plurality of memory cells, wherein the third conductive line 33 is created for the well

known and disclosed intended purpose of connecting the memory cells to other areas of the circuit.

Ikeda et al. discloses the claimed invention with the exception of forming the memory cells comprising an element programmable to multiple states of resistance.

Brickman et al. discloses in figs. 1 and 5 a method for making a memory device that comprises providing a substrate having a first conductive line 52 therein; forming a plurality of memory cells, each memory cell comprising an element **S** programmable to multiple states of resistance, wherein the memory cell comprising an element **S** programmable to multiple states of resistance is formed for the disclosed intended purpose of being used in different states by electrically altering the element when another element of the memory cell array is disabled or deactivated.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the memory cell comprising an element programmable to multiple states of resistance, wherein the element is formed as part of the memory cell for the disclosed intended purpose of being used in different states by electrically altering the element when another element of the memory cell array is disabled or deactivated as shown by Brickman et al. and as it may be applied to the invention of Ikeda et al..

Ikeda et al. further discloses forming a plurality of contacts between the first conductive line 13 and the third conductive line 33, a respective one of the plurality of

contacts being formed between respective pairs of memory cells, and forming each contact from a doped semiconductive region of the substrate.

Ikeda et al. further discloses forming a first titanium silicide layer over the first conductive line.

Regarding the limitation that the method comprises forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit and being spaced apart by a distance approximately equal to the minimum photolithographic limit, it would have been an obvious matter of design choice to form the memory cells having a width approximately equal to a minimum photolithographic limit, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to change the size of the feature as there is no statement denoting the criticality of the width of the memory cells beyond the knowledge of one of ordinary skill in the art of reducing the semiconductor features' sizes.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Ikeda et al. discloses forming dielectric spacers 15 between each pair of memory cells and forming each contact between the respective dielectric spacers, and forming the third conductive line through tapered holes extending through the dielectric material to the contacts.

Ikeda et al. further comprises disposing dielectric material on each of the plurality of memory cells.

4. Claims 20, 48, 49, and 53-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. in view of Brickman et al. and Gonzalez et al. (U. S. Pat. 5,150,276).

Ikeda et al. discloses in figs. 9, and 26-32, a method for making a memory device that comprises providing a substrate having a first conductive line 13 therein; forming a plurality of memory cells; forming a second conductive line 29, the second conductive line 29 in electrical communication with one of the memory cells; and creating a third conductive line 33 in electrical communication with the first conductive line and the plurality of memory cells, wherein the third conductive line 33 is created for the well known and disclosed intended purpose of connecting the memory cells to other areas of the circuit.

Ikeda et al. discloses the claimed invention with the exception of forming the memory cells comprising an element programmable to multiple states of resistance, the first conductive line being a digit line, forming a contact plug in an opening in the

dielectric layer, and forming a conductive line in a second conductive layer, the conductive line being in electrical communication with the contact plug..

Brickman et al. discloses in figs. 1 and 5 a method for making a memory device that comprises providing a substrate having a first conductive line 52 therein; forming a plurality of memory cells, each memory cell comprising an element **S** programmable to multiple states of resistance, wherein the memory cell comprising an element **S** programmable to multiple states of resistance is formed for the disclosed intended purpose of being used in different states by electrically altering the element when another element of the memory cell array is disabled or deactivated.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the memory cell comprising an element programmable to multiple states of resistance, wherein the element is formed as part of the memory cell for the disclosed intended purpose of being used in different states by electrically altering the element when another element of the memory cell array is disabled or deactivated as shown by Brickman et al. and as it may be applied to the invention of Ikeda et al..

Gonzalez et al. discloses in Fig. 15 and in cols. 5 to 9, a method of making a memory array, that includes forming a contact plug 175 in an insulating layer 40 wherein the memory cells are formed, forming a plurality of first conductive lines 130 disposed with one of the first conductive lines overlying and in electrical communication with a selected one of the memory cells; and forming a second

conductive line 190 in a second conductive layer, the second conductive line 190 in electrical communication with the contact plug 175, wherein Gonzalez et al. further teaches that it is well known in the art the placing of the word lines and digit lines beneath the capacitive layers (col. 2, ll. 3-21), and wherein a plurality of contact plugs are formed in the insulating layer between respective pair of memory cells, and conductive lines are formed in electrical communication with the contact plugs for the disclosed intended purpose of providing electrical communication between the contact plugs and the peripheral contacts of the cell array.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a digit line in the substrate in a multilevel structure in order to interconnect various levels of the array and to form a contact plug and a conductive line in electrical communication with the contact plug in order to provide electrical communication between the contact plug, and therefore the memory cells, and the peripheral contacts of the cell array.

Ikeda et al. further discloses forming a first titanium silicide layer over the first conductive line.

Regarding the limitation that the method comprises forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit and being spaced apart by a distance approximately equal to the minimum photolithographic limit, it would have been an obvious matter of design choice to form the memory cells having a width approximately equal to a minimum photolithographic

limit, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to change the size of the feature as there is no statement denoting the criticality of the width of the memory cells beyond the knowledge of one of ordinary skill in the art of reducing the semiconductor features' sizes.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Ikeda et al. discloses forming dielectric spacers 15 between each pair of memory cells and forming each contact between the respective dielectric spacers, and forming the third conductive line through tapered holes extending through the dielectric material to the contacts.

Ikeda et al. further comprises disposing dielectric material on each of the plurality of memory cells.

Response to Arguments

5. Applicant's arguments filed 8/9/04 have been fully considered but they are not persuasive.

Regarding applicant's argument that "Ikeda does not teach a conductive line in the substrate", it is noted that the claim language refers to "a substrate having a first conductive line therein" and that the conductive line 13 of Ikeda is within the substrate limits and bounds.

Regarding applicant's argument that the Brickman reference fails to disclose the claimed element of "a memory cell programmable to multiple states of resistance" it is noted that the claim language refers to "each said memory cell comprising an element programmable to multiple states of resistance" and that Brickman teaches within a memory cell an element that is programmable to multiple states of resistance and it is for this element that the reference is relied upon.

Regarding applicant's argument that either the Ikeda references does not teach a "third conductive line in electrical communication with said first conductive line and said plurality of memory cells" or the Ikeda reference as explained by the examiner is inoperative, as it short circuits around the memory cell, it is noted that the third conductive line 33 is in electrical communication with the conductive line 13, it is not the examiner's position or what Ikeda proposes that the conductive line 33 is in *direct electrical communication* with the conductive line 13, as seen in fig. 9, what is taught by Ikeda is that the conductive line 33 is in electrical communication with the conductive line 13 through the source electrode of the conductive line 13, there is no direct electrical communication, and the claim language does not exclude an indirect electrical communication.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571)272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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